REMARKS

Claims 1-7 and 10 are now pending in this application. The Applicant has amended claim 1. The Applicant submits that the application in now in condition for allowance. The Applicant respectfully provides the following remarks for consideration and requests the allowance of claims 1-7 and 10 in view of the remarks..

A. Rejection under 35 USC §102

The Examiner rejected claims 1-7 under 35 USC §102 as being anticipated by Knapp et al. U.S. Patent No. 5,826,072.

Claim 1, as amended, now recites that operation code comprises an event operand arranged to identify an input signal or previous event to initiate or resume processing of an event control unit and a delay operand comprising those time performance constraints executed by a counter in the event control unit. The present invention allows for the selection of what input signal will trigger the initiation or resumption of processing by the event control unit. The input signal is associated with operands that initiate or resume execution of the event control unit as well as specifies a time constraint.

The examiner claims that Knapp (US 5 826 072) teaches an instruction memory comprising time performance constraints and refers to a passage stating that a program has to be executed within a given time interval, in order to achieve that, a real time clock connected to the instruction memory is used. This is different than the present invention. In the present invention, as defined in claim 1 on the other hand, the time performance constraints are defined as operands in the instruction memory, as is more clearly defined later in the claim. No real-time clock is required. In using a real-time clock a time accuracy of microseconds to milliseconds is possible, In

using the operands of the instruction memory a time accuracy of nanoseconds can be achieved.

The examiner further claims that Knapp (US 5 826 072) teaches an instruction memory comprising events and refers to a passage describing interrupts. The difference between the conventional interrupts described in the Knapp reference and the events of the present invention, is that an interrupt causes the processor to start execution of instructions in another part of the software while the event operands of the operation code start execution of the inventive event control unit.

The applicants disagree with the viewpoint of the examiner that the event control unit could be a part of the processor that executes and/or schedules the instructions. The present invention is made on a level below the operative system and thus no scheduler handling interrupts is available. Of course, it is possible to put an operative system on top of the invention, but the invention does not require an operative system with a scheduler. This is defined in claim 1 by the inclusion of operands in the operation code defining events and delays, said operands substituting (or complementing) convention interrupt handling of the operative system. The passages of column 2 lines 25-27, column 5, line 64-column 6 line 9, column 7 lines 18-32, column 10 lines 10-14 and column 15, lines 15-21 referred to by the examiner all relate to the interrupt handling of an operative system and has nothing to do with the use of operands in the instruction memory handling events in accordance with the present claim 1. Knapp does not teach the invention as claimed in claim 1, and thus does not anticipate claim 1.

B. Rejection under 35 USC §103

The Examiner rejected claim 10under 35 USC §103 as being anticipated by Knapp et al. U.S. Patent No. 5,826,072 in view of Moorer U.S. Patent No. 4,497,023 and in further view of

Patterson et al..

As discussed above Knapp fails to teach the invention of claim 1. Peterson does not cure the deficiencies of Knapp. Peterson teaches the implementation of a superscalar processor to execute multiple instructions. Peterson however does not teach or suggest operation code comprising an event operand arranged to identify an input signal or previous event to initiate or resume processing of an event control unit and a delay operand comprising those time performance constraints executed by a counter in the event control unit as claimed in claim 1. Accordingly, the combination of Knapp and Peterson fails to teach the invention of claim 1.

CONCLUSION

All claims are believed to be in condition for allowance. If the Examiner believes that the present amendments still do not resolve all of the issues regarding patentability of the pending claims, Applicant invites the Examiner to contact the undersigned attorneys to discuss any remaining issues.. No other fees are believed to be due at this time. Should any fee be required, however, please charge such fee to Bingham McCutchen, LLP Deposit Account No. 195127, Order No. 25880.0067.

Respectfully submitted,
Bingham McCutchen, LLP

Dated: February 2, 2007 By: _____

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